DEVICE PERFORMANCE SPECIFICATION

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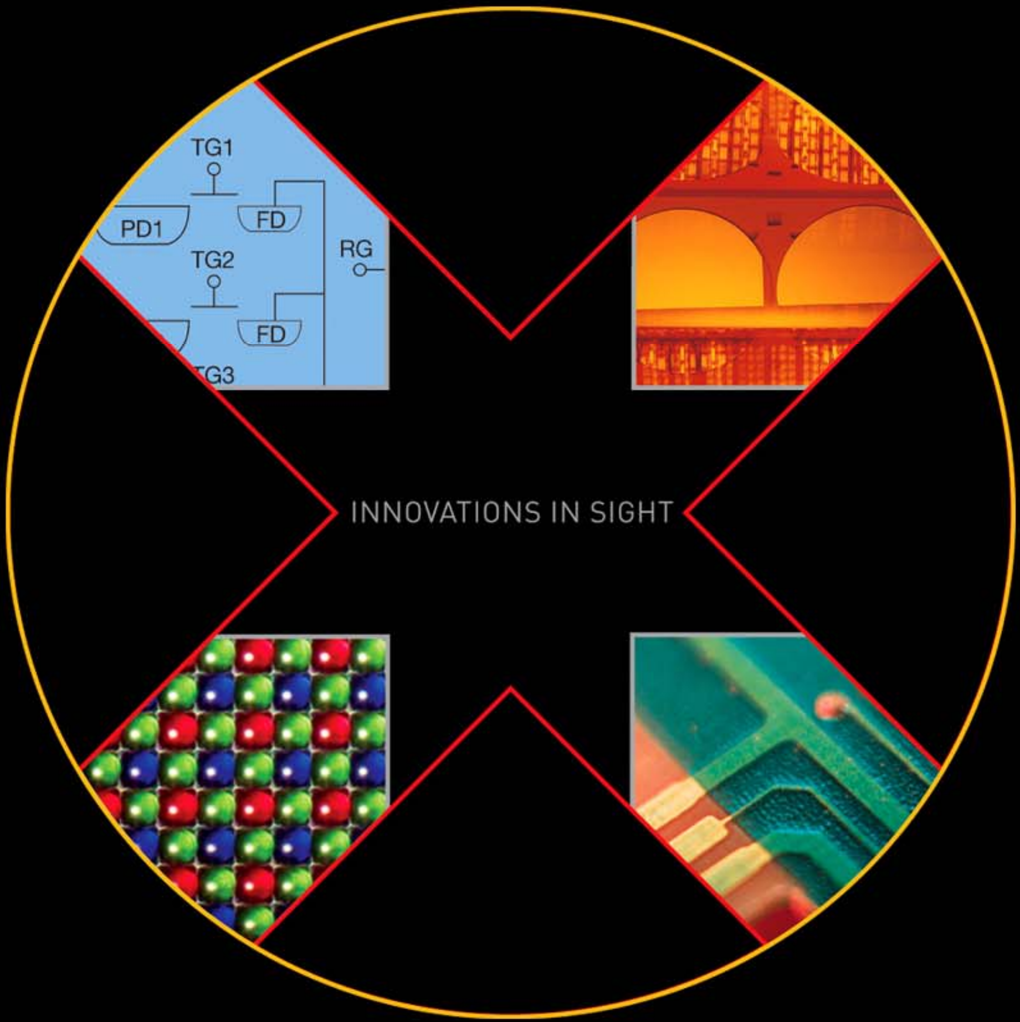
October 27, 2008



KODAK KAI-02150 IMAGE SENSOR

1920 (H) X 1080 (V) INTERLINE CCD IMAGE SENSOR

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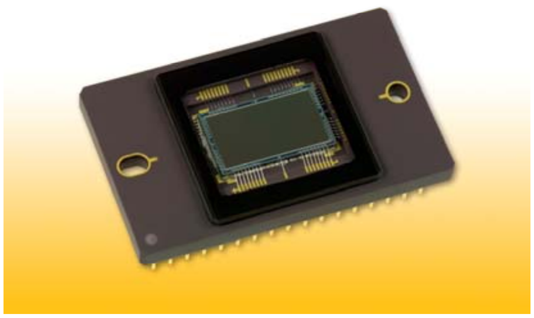
SUMMARY SPECIFICATION

KODAK KAI-02150 IMAGE SENSOR

1920 (H) X 1080 (V) PROGRESSIVE SCAN INTERLINE CCD IMAGE SENSOR

DESCRIPTION

The KODAK KAI-02150 Image Sensor is a 1920 (H) x 1080 (V) resolution, 2/3" optical format, progressive scan interline CCD. A flexible readout architecture is used that enables the use of either 1, 2 or 4 outputs to achieve frame rates up to 64 fps. The vertical overflow drain structure provides antiblooming protection and enables electronic shuttering for precise exposure control. Other features include low dark current, negligible lag and low smear.



FEATURES

- Progressive scan readout
- High frame rate
- Flexible readout architecture
- High sensitivity
- Low noise architecture
- Improved smear performance
- Electronic shutter

APPLICATIONS

- Industrial Imaging

Parameter	Typical Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	2004 (H) x 1144 (V)
Number of Effective Pixels	1960 (H) x 1120 (V)
Number of Active Pixels	1920 (H) x 1080 (V)
Pixel Size	5.5 μm (H) x 5.5 μm (V)
Active Image Size	10.56mm (H) x 5.94mm (V) 12.1mm (diagonal) 2/3" optical format
Aspect Ratio	16:9
Number of Outputs	1, 2, or 4
Charge Capacity	20,000 electrons
Output Sensitivity	34 μV/e
Quantum Efficiency KAI-02150-ABA (500nm)	50 %
Quantum Efficiency KAI-02150-CBA R(620nm), G(540nm), B(470nm)	31 %, 42 %, 43 %
Read Noise (f= 40MHz)	12 electrons rms
Dark Current	Photodiode: 7 electrons/s VCCD: 140 electrons/s
Dark Current Doubling Temperature	Photodiode: 7 °C VCCD: 9 °C
Dynamic Range	64 dB
Charge Transfer Efficiency	0.999999
Blooming Suppression	> 300 X
Smear	-100 dB
Image Lag	< 10 electrons
Maximum Pixel Clock Speed	40 MHz
Maximum Frame Rates	17 fps (single output) 33 fps (dual output) 64 fps (quad output)
Package	68 pin PGA
Cover Glass	AR Coated, 2 Sides

Unless noted, all parameters above are specified at T = 40° C

ORDERING INFORMATION

Catalog Number	Product Name	Description	Marking Code
4H2039	KAI-02150-AAA-JR-BA	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-02150-AAA Serial Number
4H2040	KAI-02150-AAA-JR-AE	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H2041	KAI-02150-ABA-JD-BA	Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-02150-ABA Serial Number
4H2042	KAI-02150-ABA-JD-AE	Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H2043	KAI-02150-ABA-JR-BA	Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass with AR coating (both sides), Standard Grade	
4H2044	KAI-02150-ABA-JR-AE	Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H2045	KAI-02150-CBA-JD-BA	Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-02150-CBA Serial Number
4H2046	KAI-02150-CBA-JD-AE	Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	

Please see ISS Application Note "Product Naming Convention" (MTD/PS-0892) for a full description of naming convention used for KODAK image sensors.

For all reference documentation, please visit our Web Site at www.kodak.com/go/imagers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010

Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

DEVICE DESCRIPTION

ARCHITECTURE

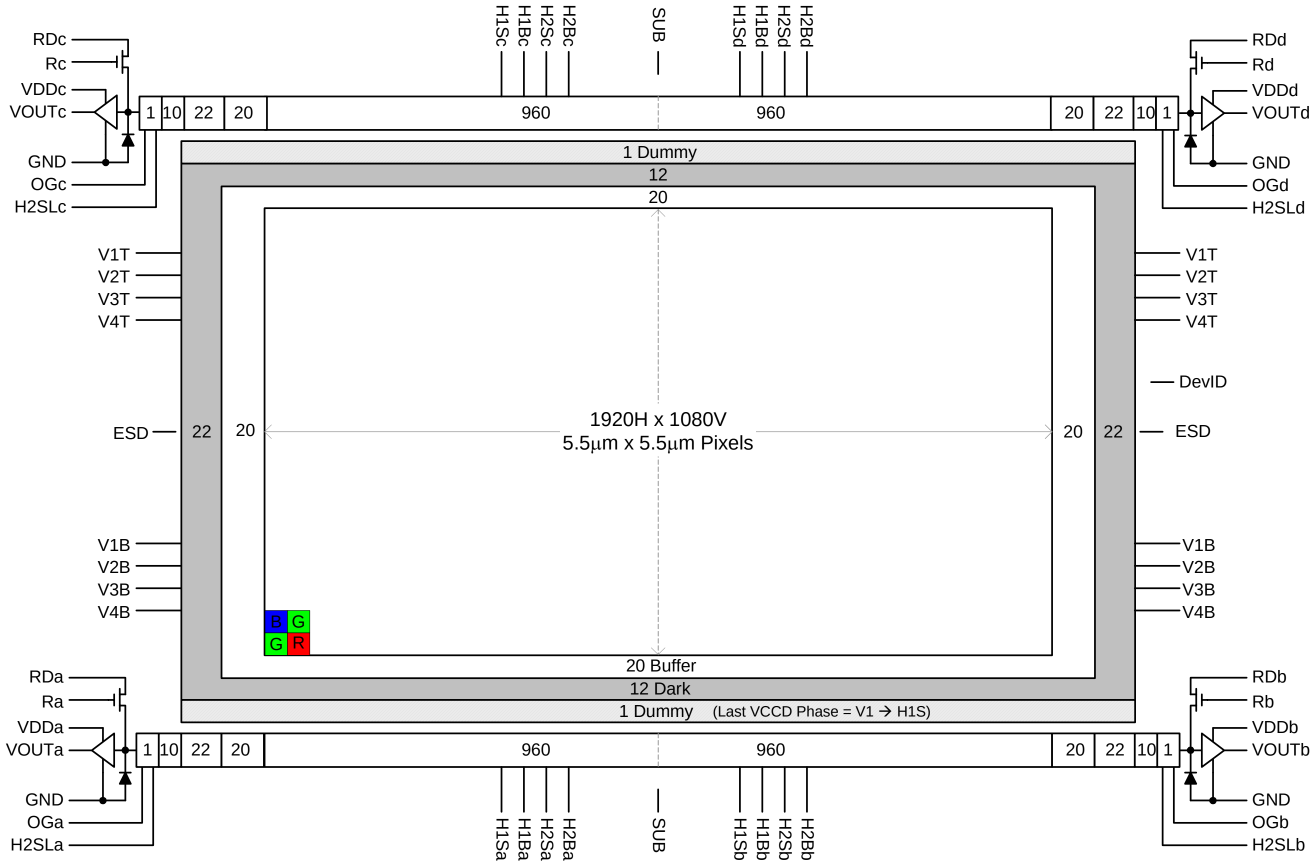


Figure 1: Block Diagram

DARK REFERENCE PIXELS

There are 12 dark reference rows at the top and 12 dark rows at the bottom of the image sensor. The dark rows are not entirely dark and so should not be used for a dark reference level. Use the 22 dark columns on the left or right side of the image sensor as a dark reference.

Under normal circumstances use only the center 20 columns of the 22 column *dark reference* due to potential light leakage.

DUMMY PIXELS

Within each horizontal shift register there are 11 leading additional shift phases. These pixels are designated as *dummy pixels* and should not be used to determine a dark reference level.

In addition, there is one dummy row of pixels at the top and bottom of the image.

ACTIVE BUFFER PIXELS

20 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as *active buffer pixels*. These pixels are light sensitive but are not tested for defects and non-uniformities.

IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependant upon light level and exposure time and non-linearly dependant on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming

ESD PROTECTION

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor. See Power Up and Power Down Sequence section.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

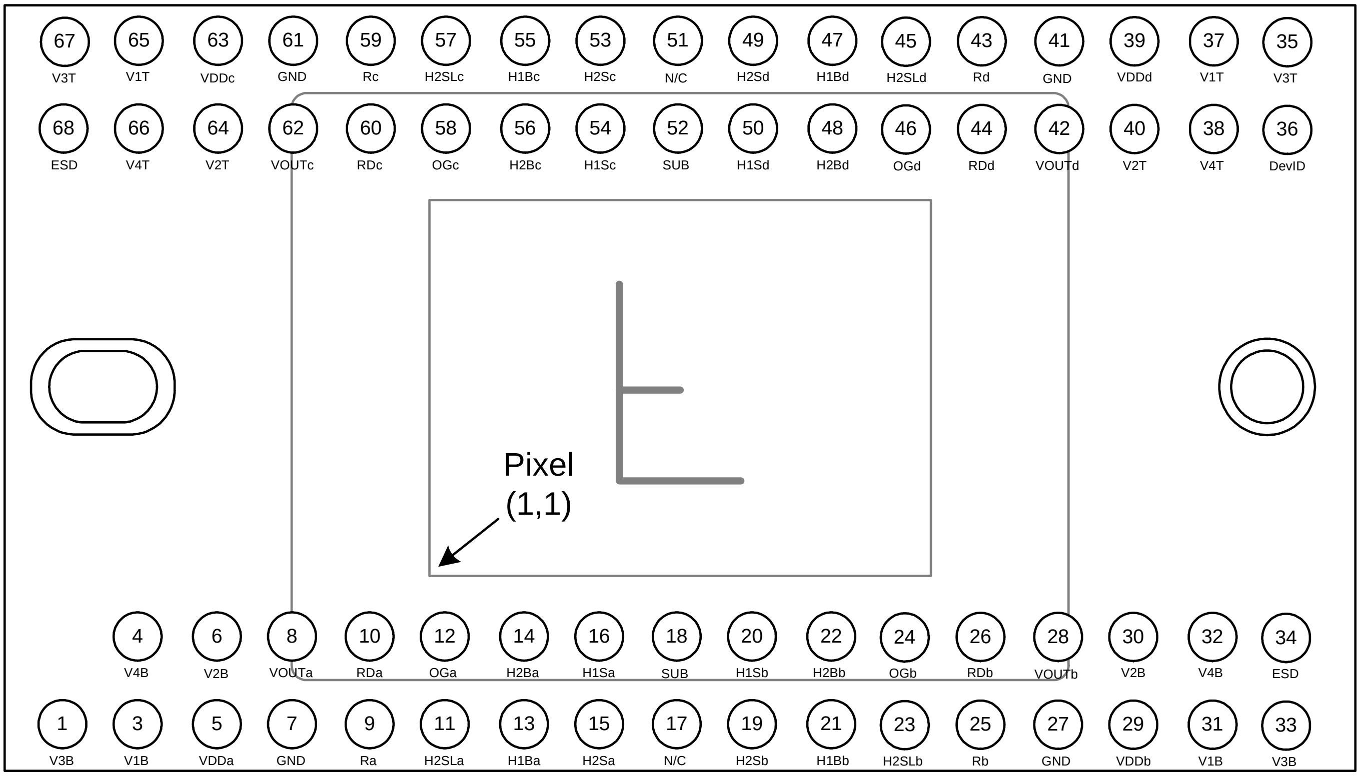


Figure 2: Package Pin Designations - Top View

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Pin	Name	Description
1	V3B	Vertical CCD Clock, Phase 3, Bottom
3	V1B	Vertical CCD Clock, Phase 1, Bottom
4	V4B	Vertical CCD Clock, Phase 4, Bottom
5	VDDa	Output Amplifier Supply, Quadrant a
6	V2B	Vertical CCD Clock, Phase 2, Bottom
7	GND	Ground
8	VOUTa	Video Output, Quadrant a
9	Ra	Reset Gate, Quadrant a
10	RDa	Reset Drain, Quadrant a
11	H2SLa	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a
12	OGa	Output Gate, Quadrant a
13	H1Ba	Horizontal CCD Clock, Phase 1, Barrier, Quadrant a
14	H2Ba	Horizontal CCD Clock, Phase 2, Barrier, Quadrant a
15	H2Sa	Horizontal CCD Clock, Phase 2, Storage, Quadrant a
16	H1Sa	Horizontal CCD Clock, Phase 1, Storage, Quadrant a
17	N/C	No Connect
18	SUB	Substrate
19	H2Sb	Horizontal CCD Clock, Phase 2, Storage, Quadrant b
20	H1Sb	Horizontal CCD Clock, Phase 1, Storage, Quadrant b
21	H1Bb	Horizontal CCD Clock, Phase 1, Barrier, Quadrant b
22	H2Bb	Horizontal CCD Clock, Phase 2, Barrier, Quadrant b
23	H2SLb	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant b
24	OGb	Output Gate, Quadrant b
25	Rb	Reset Gate, Quadrant b
26	RDb	Reset Drain, Quadrant b
27	GND	Ground
28	VOUTb	Video Output, Quadrant b
29	VDDb	Output Amplifier Supply, Quadrant b
30	V2B	Vertical CCD Clock, Phase 2, Bottom
31	V1B	Vertical CCD Clock, Phase 1, Bottom
32	V4B	Vertical CCD Clock, Phase 4, Bottom
33	V3B	Vertical CCD Clock, Phase 3, Bottom
34	ESD	ESD Protection Disable

Pin	Name	Description
68	ESD	ESD Protection Disable
67	V3T	Vertical CCD Clock, Phase 3, Top
66	V4T	Vertical CCD Clock, Phase 4, Top
65	V1T	Vertical CCD Clock, Phase 1, Top
64	V2T	Vertical CCD Clock, Phase 2, Top
63	VDDc	Output Amplifier Supply, Quadrant c
62	VOUTc	Video Output, Quadrant c
61	GND	Ground
60	RDc	Reset Drain, Quadrant c
59	Rc	Reset Gate, Quadrant c
58	OGc	Output Gate, Quadrant c
57	H2SLc	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c
56	H2Bc	Horizontal CCD Clock, Phase 2, Barrier, Quadrant c
55	H1Bc	Horizontal CCD Clock, Phase 1, Barrier, Quadrant c
54	H1Sc	Horizontal CCD Clock, Phase 1, Storage, Quadrant c
53	H2Sc	Horizontal CCD Clock, Phase 2, Storage, Quadrant c
52	SUB	Substrate
51	N/C	No Connect
50	H1Sd	Horizontal CCD Clock, Phase 1, Storage, Quadrant d
49	H2Sd	Horizontal CCD Clock, Phase 2, Storage, Quadrant d
48	H2Bd	Horizontal CCD Clock, Phase 2, Barrier, Quadrant d
47	H1Bd	Horizontal CCD Clock, Phase 1, Barrier, Quadrant d
46	OGd	Output Gate, Quadrant b
45	H2SLd	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d
44	RDd	Reset Drain, Quadrant d
43	Rd	Reset Gate, Quadrant d
42	VOUTd	Video Output, Quadrant d
41	GND	Ground
40	V2T	Vertical CCD Clock, Phase 2, Top
39	VDDd	Output Amplifier Supply, Quadrant d
38	V4T	Vertical CCD Clock, Phase 4, Top
37	V1T	Vertical CCD Clock, Phase 1, Top
36	DevID	Device Identification
35	V3T	Vertical CCD Clock, Phase 3, Top

Notes:
Liked named pins are internally connected and should have a common drive signal.
N/C pins (17, 51) should be left floating.

IMAGING PERFORMANCE

TYPICAL OPERATION CONDITIONS

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

Description	Condition	Notes
Light Source	Continuous red, green and blue LED illumination	1
Operation	Nominal operating voltages and timing	

Notes:
1. For monochrome sensor, only green LED used.

SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes	Test
Dark Field Global Non-Uniformity	DSNU	-	-	2.0	mVpp	Die	27, 40		1
Bright Field Global Non-Uniformity		-	2.0	5.0	%rms	Die	27, 40	1	2
Bright Field Global Peak to Peak Non-Uniformity	PRNU	-	5.0	15.0	%pp	Die	27, 40	1	3
Bright Field Center Non-Uniformity		-	1.0	2.0	%rms	Die	27, 40	1	4
Maximum Photoresponse Nonlinearity	NL	-	2	-	%	Design		2	
Maximum Gain Difference Between Outputs	ΔG	-	10	-	%	Design		2	
Maximum Signal Error due to Nonlinearity Differences	ΔNL	-	1	-	%	Design		2	
Horizontal CCD Charge Capacity	HNe	-	55	-	ke^-	Design			
Vertical CCD Charge Capacity	VNe	-	45	-	ke^-	Design			
Photodiode Charge Capacity	PNe	-	20	-	ke^-	Die	27, 40	3	
Horizontal CCD Charge Transfer Efficiency	HCTE	0.999995	0.999999	-		Die			
Vertical CCD Charge Transfer Efficiency	VCTE	0.999995	0.999999	-		Die			
Photodiode Dark Current	Ipd	-	7	70	e/p/s	Die	40		
Vertical CCD Dark Current	Ivd	-	140	400	e/p/s	Die	40		
Image Lag	Lag	-	-	10	e^-	Design			
Antiblooming Factor	Xab	300	-	-		Design			
Vertical Smear	Smr	-	-100	-	dB	Design			
Read Noise	n_{e-T}	-	12	-	e^-rms	Design		4	
Dynamic Range	DR	-	64	-	dB	Design		4, 5	
Output Amplifier DC Offset	V_{odc}	-	9.4	-	V	Die	27, 40		
Output Amplifier Bandwidth	f_{-3db}	-	250	-	MHz	Die		6	
Output Amplifier Impedance	R_{OUT}	-	127	-	Ohms	Die	27, 40		
Output Amplifier Sensitivity	$\Delta V/\Delta N$	-	34	-	$\mu V/e^-$	Design			

KAI-02150-ABA

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes	Test
Peak Quantum Efficiency	QE_{max}	-	50	-	%	Design			
Peak Quantum Efficiency Wavelength	λQE	-	500	-	nm	Design			

KAI-02150-CBA

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes	Test
Peak Quantum Efficiency Blue Green Red	QE_{max}	-	43 42 31	-	%	Design			
Peak Quantum Efficiency Wavelength Blue Green Red	λQE	-	470 540 620	-	nm	Design			

Notes:
1. Per color
2. Value is over the range of 10% to 90% of photodiode saturation.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is 680 mV.
4. At 40 MHz.
5. Uses 20LOG(PNe/ n_{e-T})
6. Assumes 5pF load

TYPICAL PERFORMANCE CURVES

QUANTUM EFFICIENCY

Monochrome with Microlens

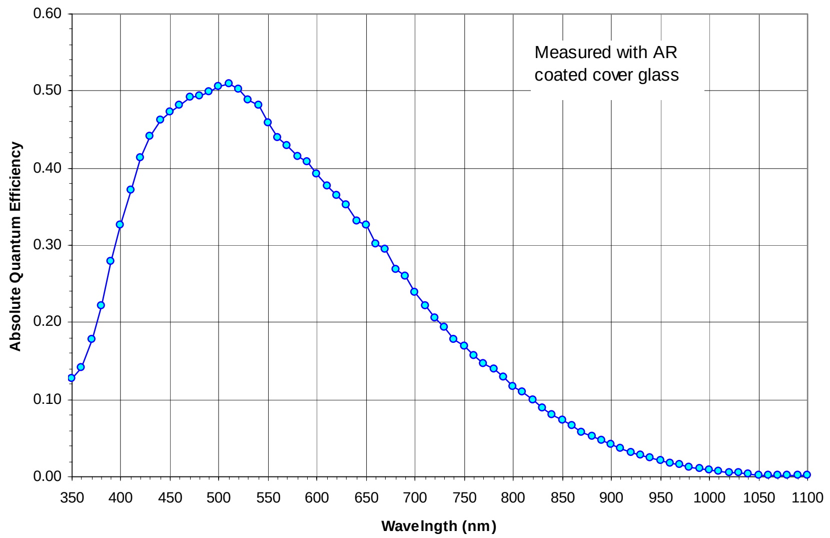


Figure 3: Monochrome with Microlens Quantum Efficiency

Monochrome without Microlens

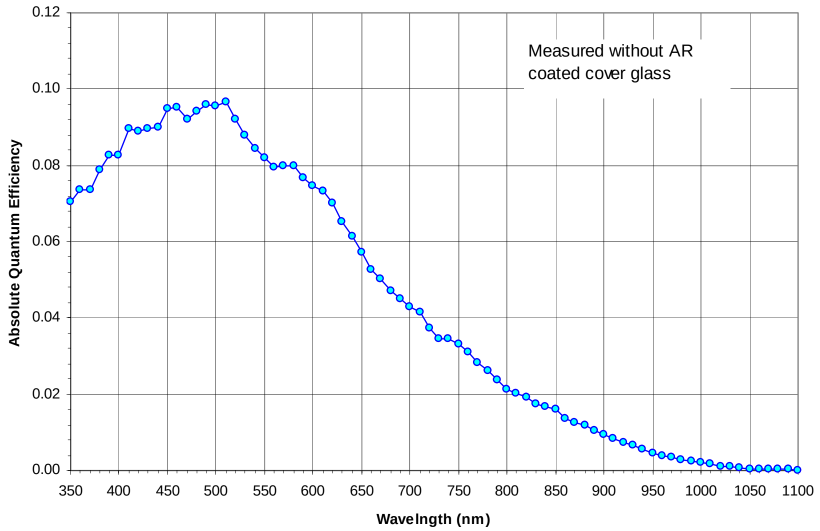


Figure 4: Monochrome without Microlens Quantum Efficiency

Color (Bayer RGB) with Microlens

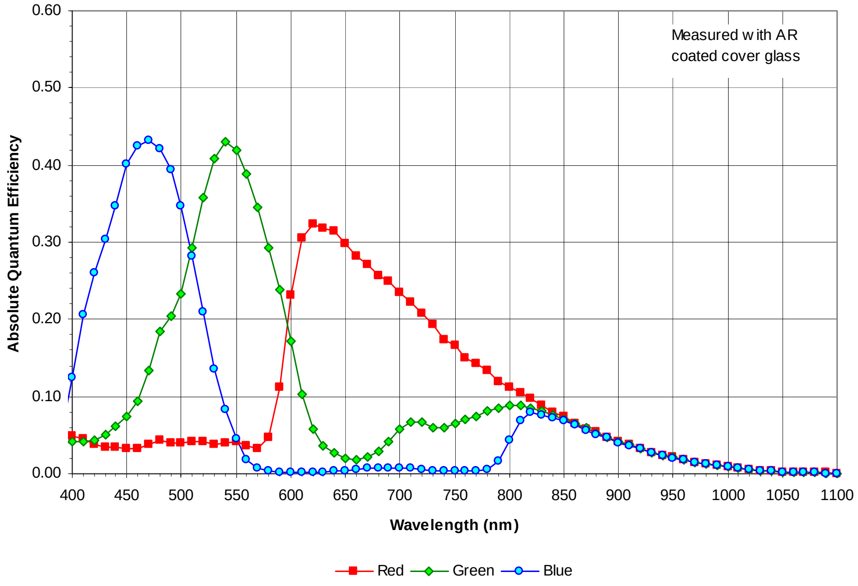


Figure 5: Color with Microlens Quantum Efficiency

ANGULAR QUANTUM EFFICIENCY

For the curves marked "Horizontal", the incident light angle is varied in a plane parallel to the HCCD.
For the curves marked "Vertical", the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

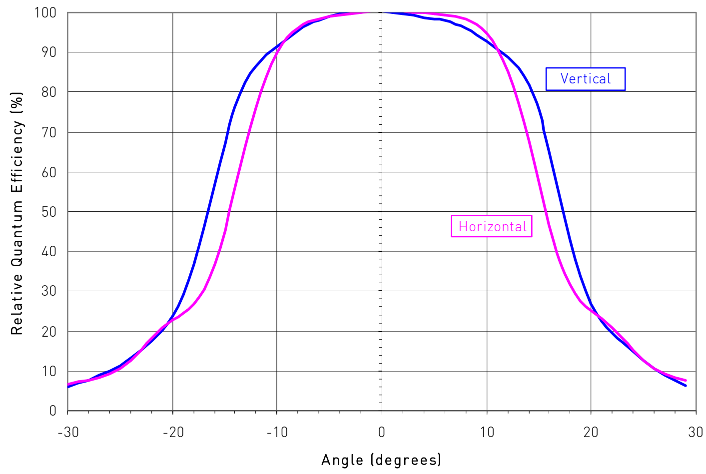


Figure 6: Monochrome with Microlens Angular Quantum Efficiency

DARK CURRENT VERSUS TEMPERATURE

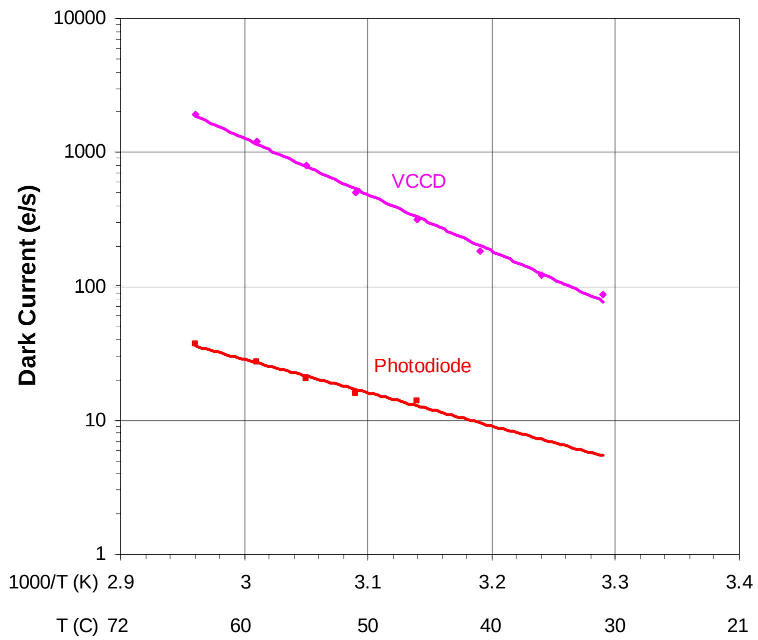


Figure 7: Dark Current versus Temperature

POWER – ESTIMATED

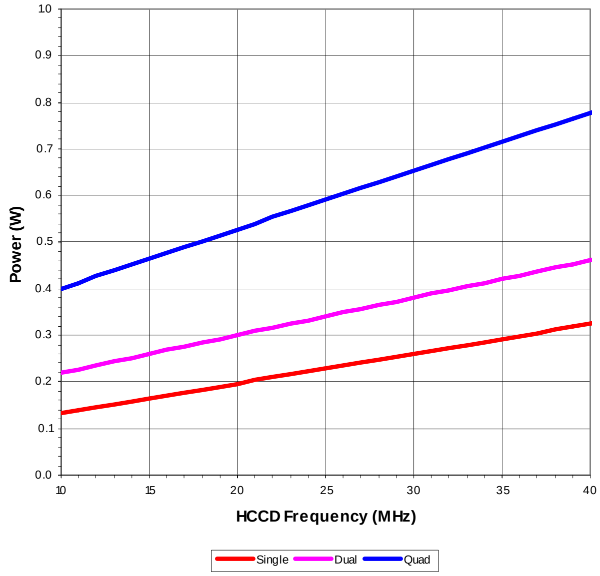


Figure 8: Power

FRAME RATES

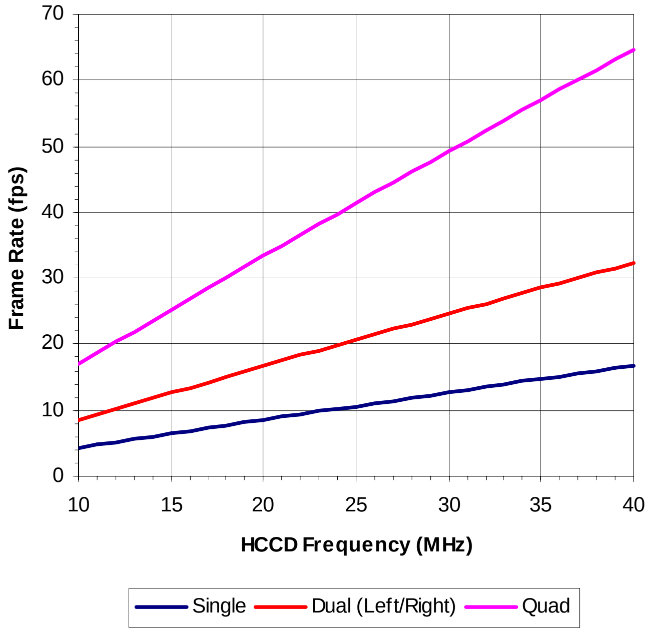


Figure 9: Frame Rates

DEFECT DEFINITIONS

OPERATION CONDITIONS FOR DEFECT TESTING AT 40°C

Description	Condition	Notes
Operational Mode	Two outputs, using VOUTa and VOUTc, continuous readout	
HCCD Clock Frequency	10 MHz	
Pixels Per Line	2160	1
Lines Per Frame	672	2
Line Time	218.9 μsec	
Frame Time	147.1 msec	
Photodiode Integration Time	Mode A: PD_Tint = Frame Time = 147.1 msec, no electronic shutter used Mode B: PD_Tint = 33 msec, electronic shutter used	
VCCD Integration Time	125.2 msec	3
Temperature	40°C	
Light Source	Continuous red, green and blue LED illumination	4
Operation	Nominal operating voltages and timing	

Notes
1. Horizontal overclocking used
2. Vertical overclocking used
3. VCCD Integration Time = 572 lines x Line Time, which is the total time a pixel will spend in the VCCD registers.
4. For monochrome sensor, only the green LED is used.

DEFECT DEFINITIONS FOR TESTING AT 40°C

Description	Definition	Standard Grade	Notes	Test
Major dark field defective bright pixel	PD_Tint = Mode A -> Defect >= 51 mV or PD_Tint = Mode B -> Defect >= 12 mV	20	1	5
Major bright field defective dark pixel	Defect >= 12 %			6
Minor dark field defective bright pixel	PD_Tint = Mode A -> Defect >= 26 mV or PD_Tint = Mode B -> Defect >= 6 mV	200		
Cluster Defect	A group of 2 to 10 contiguous major defective pixels	8	2	
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	2	

Notes:
1. For the color device (KAI-02150-CBA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

OPERATION CONDITIONS FOR DEFECT TESTING AT 27°C

Description	Condition	Notes
Operational Mode	Two outputs, using VOUTa and VOUTc, continuous readout	
HCCD Clock Frequency	20 MHz	
Pixels Per Line	2160	1
Lines Per Frame	672	2
Line Time	109.8 μsec	
Frame Time	73.8 msec	
Photodiode Integration Time (PD_Tint)	Mode A: PD_Tint = Frame Time = 73.8.2 msec, no electronic shutter used	
	Mode B: PD_Tint = 33 msec, electronic shutter used	
VCCD Integration Time	62.8 msec	3
Temperature	27°C	
Light Source	Continuous red, green and blue LED illumination	4
Operation	Nominal operating voltages and timing	

Notes
1. Horizontal overclocking used
2. Vertical overclocking used
3. VCCD Integration Time = 572 lines x Line Time, which is the total time a pixel will spend in the VCCD registers.
4. For monochrome sensor, only the green LED is used.

DEFECT DEFINITIONS FOR TESTING AT 27°C

Description	Definition	Standard Grade	Notes	Test
Major dark field defective bright pixel	PD_Tint = Mode A -> Defect >= 8 mV or PD_Tint = Mode B -> Defect >= 4 mV	20	1	5
Major bright field defective dark pixel	Defect >= 12 %			6
Cluster Defect	A group of 2 to 10 contiguous major defective pixels	8	2	
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	2	

Notes:
1. For the color device (KAI-02150-CBA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27C) temperature. Minor point defects are not included in the defect map. All defective pixels are reference to pixel 1,1 in the defect maps. See Figure 10: Regions of Interest for the location of pixel 1,1.

TEST DEFINITIONS

TEST REGIONS OF INTEREST

```
Image Area ROI:    Pixel   1,   1 to Pixel 1960, 1120
Active Area ROI:   Pixel  21,  21 to Pixel 1940, 1100
Center ROI:        Pixel 931, 511 to Pixel 1030,  610
```

Only the Active Area ROI pixels are used for performance and defect tests.

OVERCLOCKING

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 10 for a pictorial representation of the regions of interest.

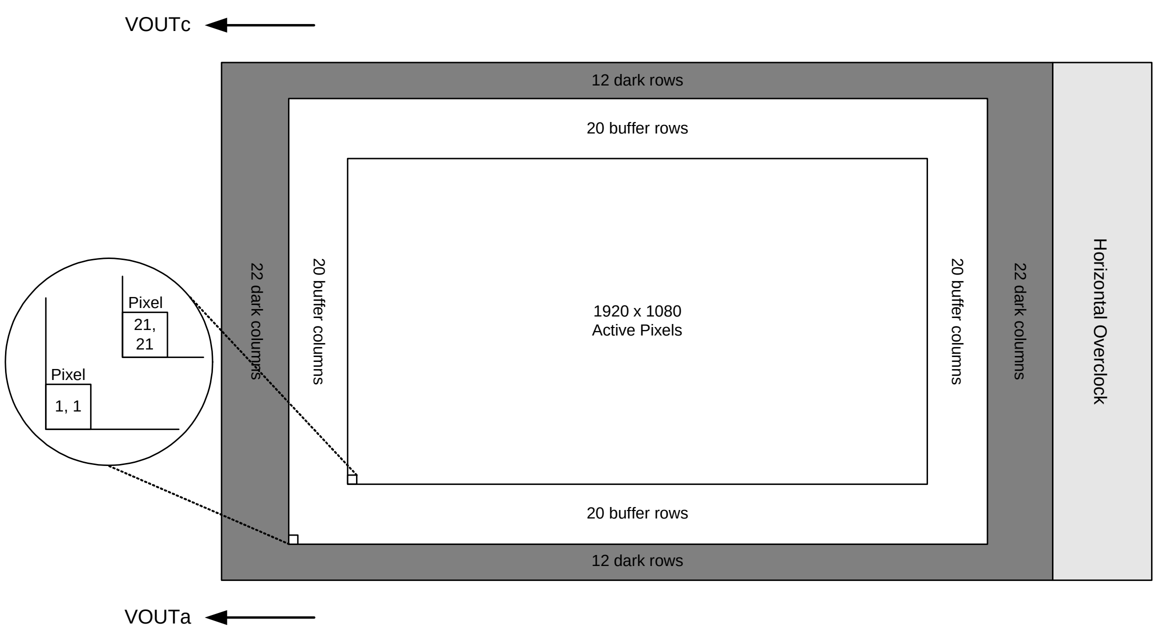


Figure 10: Regions of Interest

TESTS

1. Dark Field Global Non-Uniformity

This test is performed under dark field conditions. The sensor is partitioned into 144 sub regions of interest, each of which is 120 by 120 pixels in size. See Figure 11: Test Sub Regions of Interest. The average signal level of each of the 144 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in counts – Horizontal overclock average in counts) * mV per count
Where i = 1 to 144. During this calculation on the 144 sub regions of interest, the maximum and minimum signal levels are found.

The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

Units: mVpp (millivolts peak to peak)

2. Global Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. Global non-uniformity is defined as

$$\text{Global Non-Uniformity} = 100 * \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}} \right) \quad \text{Units: \%rms}$$

Active Area Signal = Active Area Average – Dark Column Average

3. Global Peak to Peak Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. The sensor is partitioned into 144 sub regions of interest, each of which is 120 by 120 pixels in size. See Figure 11: Test Sub Regions of Interest. The average signal level of each of the 144 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in counts – Horizontal overclock average in counts) * mV per count
Where i = 1 to 144. During this calculation on the 144 sub regions of interest, the maximum and minimum signal levels are found.

The global peak to peak uniformity is then calculated as:

$$\text{Global Uniformity} = 100 * \frac{\text{Maximum Signal - Minimum Signal}}{\text{Active Area Signal}}$$

Units: %pp

4. Center Non-Uniformity
This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels of the sensor. Center uniformity is defined as:

$$\text{Center ROI Uniformity} = 100 * \left(\frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}} \right)$$

Units: %rms
Center ROI Signal = Center ROI Average – Dark Column Average

5. Dark field defect test
This test is performed under dark field conditions. The sensor is partitioned into 144 sub regions of interest, each of which is 120 by 120 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the “Defect Definitions” section.

6. Bright field defect test
This test is performed with the imager illuminated to a level such that the output is at approximately 476 mV. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal * threshold
Bright defect threshold = Active Area Signal * threshold

The sensor is then partitioned into 144 sub regions of interest, each of which is 120 by 120 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.
Example for major bright field defective pixels:

- Average value of all active pixels is found to be 476 mV
- Dark defect threshold: 476 mV * 12 % = 57 mV
- Bright defect threshold: 476 mV * 12 % = 57 mV
- Region of interest #1 selected. This region of interest is pixels 21,21 to pixels 140, 140.
    - Median of this region of interest is found to be 470 mV.
    - Any pixel in this region of interest that is >= (470 + 57 mV) 527 mV in intensity will be marked defective.
    - Any pixel in this region of interest that is <= (470 - 57 mV) 413 mV in intensity will be marked defective.

All remaining 144 sub regions of interest are analyzed for defective pixels in the same manner.

Test Sub Regions of Interest

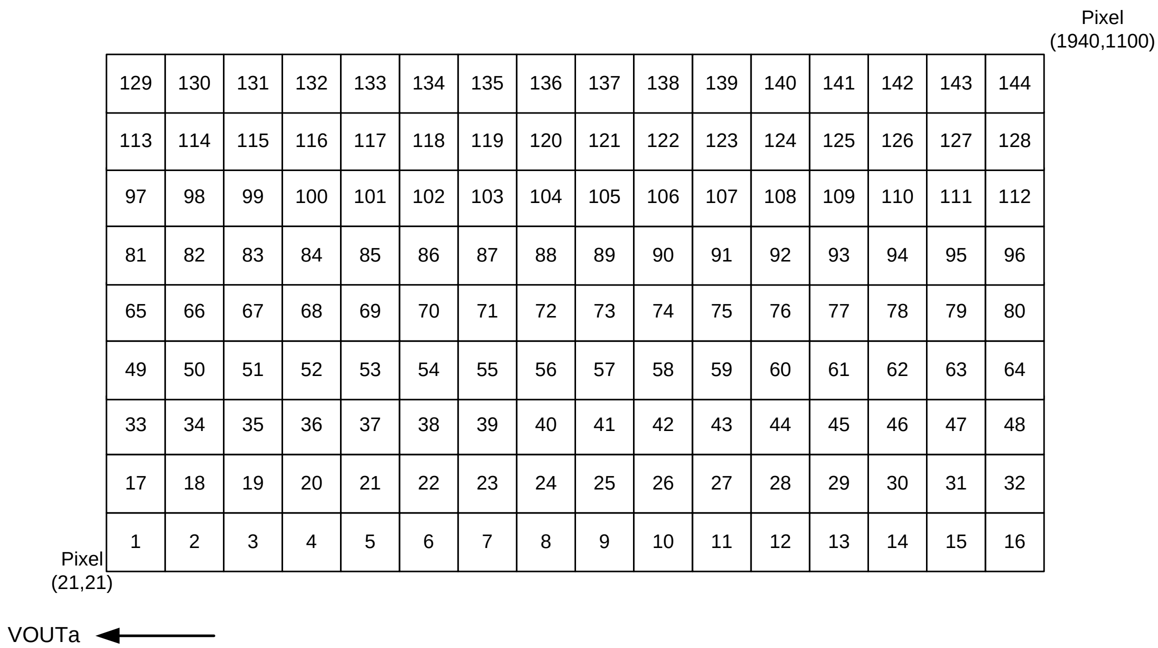


Figure 11: Test Sub Regions of Interest

OPERATION

ABSOLUTE MAXIMUM RATINGS

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged. Operation at these values will reduce MTTF.

Description	Symbol	Minimum	Maximum	Units	Notes
Operating Temperature	T_{OP}	-50	+70	°C	1
Humidity	RH	+5	+90	%	2
Output Bias Current	Iout	-	60	mA	3
Off-chip Load	C_L	-	10	pF	

Notes:
1. Noise performance will degrade at higher temperatures.
2. T=25ºC. Excessive humidity will degrade MTTF.
3. Total for all outputs. Maximum current is -15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND

Description	Minimum	Maximum	Units	Notes
VDDα, VOUTα, RDα	-0.4	17.5	V	1
V1B, V1T	ESD – 0.4	ESD + 24.0	V	
V2B, V2T, V3B, V3T, V4B, V4T	ESD – 0.4	ESD + 14.0	V	
H1Sα, H1Bα, H2Sα, H2Bα, H2SLα, Rα, OGα	ESD – 0.4	ESD + 14.0	V	1
ESD	-10.0	0.0	V	
SUB	-0.4	40.0	V	

Notes:
1. α denotes a, b, c or d

POWER UP AND POWER DOWN SEQUENCE

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor.

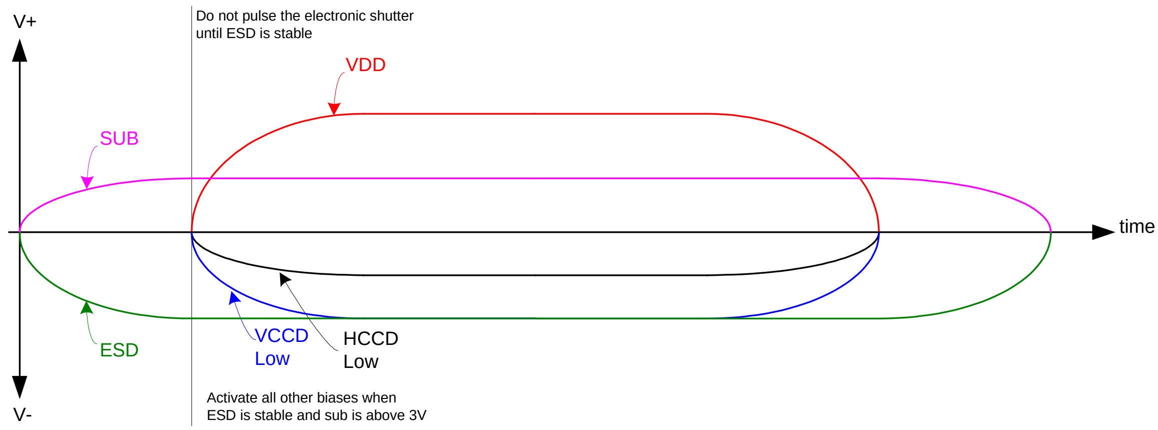
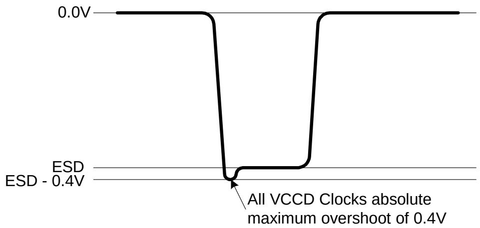


Figure 12: Power Up and Power Down Sequence

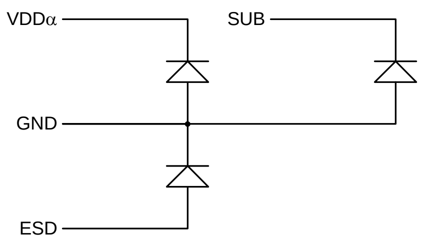
Notes:

1. Activate all other biases when ESD is stable and SUB is above 3V
2. Do not pulse the electronic shutter until ESD is stable
3. VDD cannot be +15V when SUB is 0V
4. The image sensor can be protected from an accidental improper ESD voltage by current limiting the SUB current to less than 10mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect the sensor from accidental overshoots of SUB, VDD and ESD during power on and power off. See the figure below.

The VCCD clock waveform must not have a negative overshoot more than 0.4V below the ESD voltage.



Example of external diode protection for SUB, VDD and ESD.
α denotes a, b, c or d



DC BIAS OPERATING CONDITIONS

Description	Pins	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current	Notes
Reset Drain	RDα	RD	+11.8	+12.0	+12.2	V	10μA	1
Output Gate	OGα	OG	-2.2	-2.0	-1.8	V	10μA	1
Output Amplifier Supply	VDDα	VDD	+14.5	+15.0	+15.5	V	11.0 mA	1, 2
Ground	GND	GND	0.0	0.0	0.0	V	-1.0 mA	
Substrate	SUB	VSUB	+5.0	VAB	VDD	V	50μA	3
ESD Protection Disable	ESD	ESD	-9.5	-9.0	-8.8	V	50μA	6, 7
Output Bias Current	VOUTα	Iout	-3.0	-7.0	-10.0	mA	——	1, 4, 5

Notes:
1. α denotes a, b, c or d
2. The maximum DC current is for one output. Idd = Iout + Iss. See Figure 13.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is the nominal PNe (see Specifications).
4. An output load sink must be applied to each VOUT pin to activate each output amplifier.
5. Nominal value required for 40MHz operation per output. May be reduced for slower data rates and lower noise.
6. Adherence to the power-up and power-down sequence is critical. See Power Up and Power Down Sequence section.
7. ESD maximum value must be less than or equal to V1_L+0.4V and V2_L+0.4V

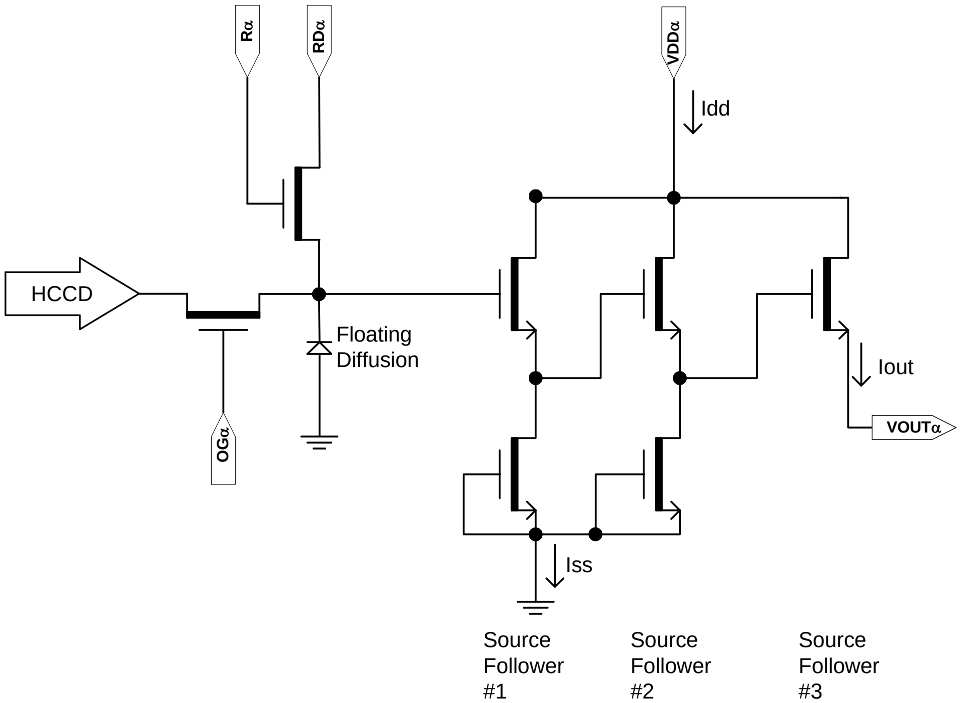


Figure 13: Output Amplifier

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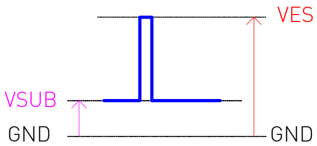
AC OPERATING CONDITIONS

Clock Levels

Description	Pins[1]	Symbol	Level	Minimum	Nominal	Maximum	Units	Capacitance[2]
Vertical CCD Clock, Phase 1	V1B, V1T	V1_L	Low	-9.5	-9.0	-8.5	V	12nF
		V1_M	Mid	-0.2	+0.0	+0.2		
		V1_H	High	+11.5	+12.0	+12.5		
Vertical CCD Clock, Phase 2	V2B, V2T	V2_L	Low	-9.5	-9.0	-8.5	V	12nF
		V2_H	High	-0.2	+0.0	+0.2		
Vertical CCD Clock, Phase 3	V3B, V3T	V3_L	Low	-9.5	-9.0	-8.5	V	12nF
		V3_H	High	-0.2	+0.0	+0.2		
Vertical CCD Clock, Phase 4	V4B, V4T	V4_L	Low	-9.5	-9.0	-8.5	V	12nF
		V4_H	High	-0.2	+0.0	+0.2		
Horizontal CCD Clock, Phase 1 Storage	H1Sα	H1S_L	Low	-4.2	-4.0	-3.8	V	170pF
		H1S_A	Amplitude	+3.8	+4.0	+5.0		
Horizontal CCD Clock, Phase 1 Barrier	H1Bα	H1B_L	Low	-4.2	-4.0	-3.8	V	110pF
		H1B_A	Amplitude	+3.8	+4.0	+5.0		
Horizontal CCD Clock, Phase 2 Storage	H2Sα	H2S_L	Low	-4.2	-4.0	-3.8	V	170pF
		H2S_A	Amplitude	+3.8	+4.0	+5.0		
Horizontal CCD Clock, Phase 2 Barrier	H2Bα	H2B_L	Low	-5.2	-4.0	-3.8	V	110pF
		H2B_A	Amplitude	+3.8	+4.0	+5.4		
Horizontal CCD Clock, Last Phase[3]	H2SLα	H2SL_L	Low	-5.2	-5.0	-4.8	V	20pF
		H2SL_A	Amplitude	+4.8	+5.0	+5.2		
Reset Gate	Rα	R_L[4]	Low	-3.5	-2.0	-1.5	V	16pF
		R_H	High	+2.5	+3.0	+4.0		
Electronic Shutter	SUB	VES	High	+29.0	+30.0	+40.0	V	800pF

Notes:
1. α denotes a, b, c or d
2. Capacitance is total for all like named pins
3. Use separate clock driver for improved speed performance.
4. Reset low should be set to –3 volts for signal levels greater than 40,000 electrons.

The figure below shows the DC bias (VSUB) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.



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DEVICE IDENTIFICATION

The device identification pin (DevID) may be used to determine which Kodak 5.5 micron pixel interline CCD sensor is being used.

Description	Pins	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current	Notes
Device Identification	DevID	DevID	49,000	55,000	61,000	Ohms	TBD	1, 2, 3

Notes:

1. Nominal value subject to verification and/or change during release of preliminary specifications.
2. If the Device Identification is not used, it may be left disconnected.
3. After Device Identification resistance has been read during camera initialization, it is recommended that the circuit be disabled to prevent localized heating of the sensor due to current flow through the R_DeviceID resistor.

Recommended Circuit

Note that V1 must be a different value than V2.

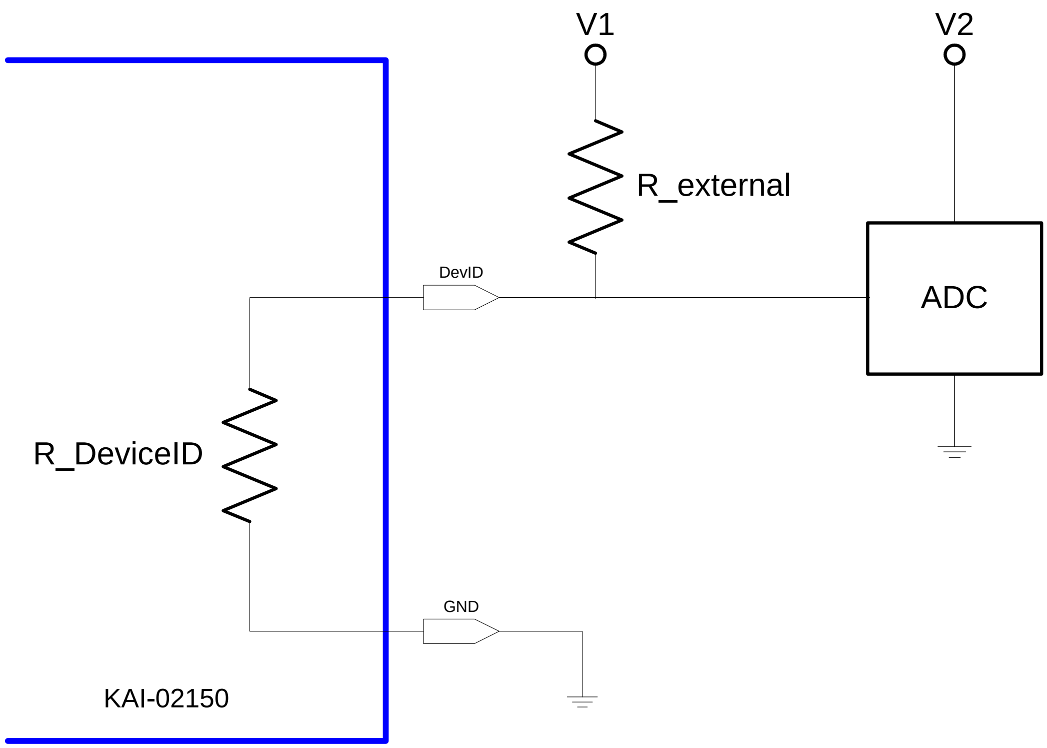

Figure 14: Device Identification Recommended Circuit

TIMING

REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Photodiode Transfer	t_{pd}	1.0	-	-	µs	
VCCD Leading Pedestal	t_{3p}	4.0	-	-	µs	
VCCD Trailing Pedestal	t_{3d}	4.0	-	-	µs	
VCCD Transfer Delay	t_d	1.0	-	-	µs	
VCCD Transfer	t_v	1.0	-	-	µs	
VCCD Clock Cross-over	v_{VCR}	50	75	100	%	
HCCD Delay	t_{hs}	0.2	-	-	µs	
HCCD Transfer	t_e	25.0	-	-	ns	
Shutter Transfer	t_{sub}	1.0	-	-	µs	
Shutter Delay	t_{hd}	1.0	-	-	µs	
Reset Pulse	t_r	2.5	-	-	ns	
Reset – Video Delay	t_{rv}	-	2.2	-	ns	
H2SL – Video Delay	t_{hv}	-	3.1	-	ns	
Line Time	t_{line}	27.0	-	-	µs	Dual HCCD Readout
		52.1	-	-		Single HCCD Readout
Frame Time	t_{frame}	64.6	-	-	ms	Quad HCCD Readout
		32.3	-	-		Dual HCCD Readout
		16.8	-	-		Single HCCD Readout

Notes:
Refer to timing diagrams as shown in Figure 15, Figure 16, Figure 17, Figure 18 and Figure 19

TIMING DIAGRAMS

The timing sequence for the clocked device pins may be represented as one of seven patterns (P1-P7) as shown in the table below. The patterns are defined in Figure 15 and Figure 16. Contact Image Sensor Solutions Application Engineering for other readout modes.

Device Pin	Readout Patterns: Quad	Readout Patterns: Dual VOUTa, VOUTb	Readout Patterns: Dual VOUTa, VOUTc	Readout Patterns: Single VOUTa
V1T	P1T	P1B	P1T	P1B
V2T	P2T	P4B	P2T	P4B
V3T	P3T	P3B	P3T	P3B
V4T	P4T	P2B	P4T	P2B
V1B	P1B			
V2B	P2B			
V3B	P3B			
V4B	P4B			
H1Sa	P5			
H1Ba				
H2Sa[2]	P6			
H2Ba				
Ra	P7			
H1Sb	P5		P5	
H1Bb			P6	
H2Sb[2]	P6		P6	
H2Bb			P5	
Rb	P7		P7[1] or Off[3]	P7[1] or Off[3]
H1Sc	P5	P5[1] or Off[3]	P5	P5[1] or Off[3]
H1Bc				
H2Sc[2]	P6	P6[1] or Off[3]	P6	P6[1] or Off[3]
H2Bc				
Rc	P7	P7[1] or Off[3]	P7	P7[1] or Off[3]
H1Sd	P5	P5[1] or Off[3]	P5	P5[1] or Off[3]
H1Bd			P6	
H2Sd[2]	P6	P6[1] or Off[3]	P6	P6[1] or Off[3]
H2Bd			P5	
Rd	P7	P7[1] or Off[3]	P7[1] or Off[3]	P7[1] or Off[3]

# Lines/Frame (Minimum)	572	1144	572	1144
# Pixels/Line (Minimum)	1013		2026	

Notes:

1. For optimal performance of the sensor. May be clocked at a lower frequency. If clocked at a lower frequency, the frequency selected should be a multiple of the frequency used on the a and b register.
2. H2SLx follows the same pattern as H2Sx For optimal speed performance, use a separate clock driver.
3. Off = +5V. Note that there may be operating conditions (high temperature and/or very bright light sources) that will cause blooming from the unused c/d register into the image area.

Photodiode Transfer Timing

A row of charge is transferred to the HCCD on the falling edge of V1 as indicated in the P1 pattern below. Using this timing sequence, the leading dummy row or line is combined with the first dark row in the HCCD. The "Last Line" is dependant on readout mode – either 572 or 1144 minimum counts required. It is important to note that, in general, the rising edge of a vertical clock (patterns P1-P4) should be coincident or slightly leading a falling edge at the same time interval. This is particularly true at the point where P1 returns from the high (3rd level) state to the mid state when P4 transitions from the low state to the high state.

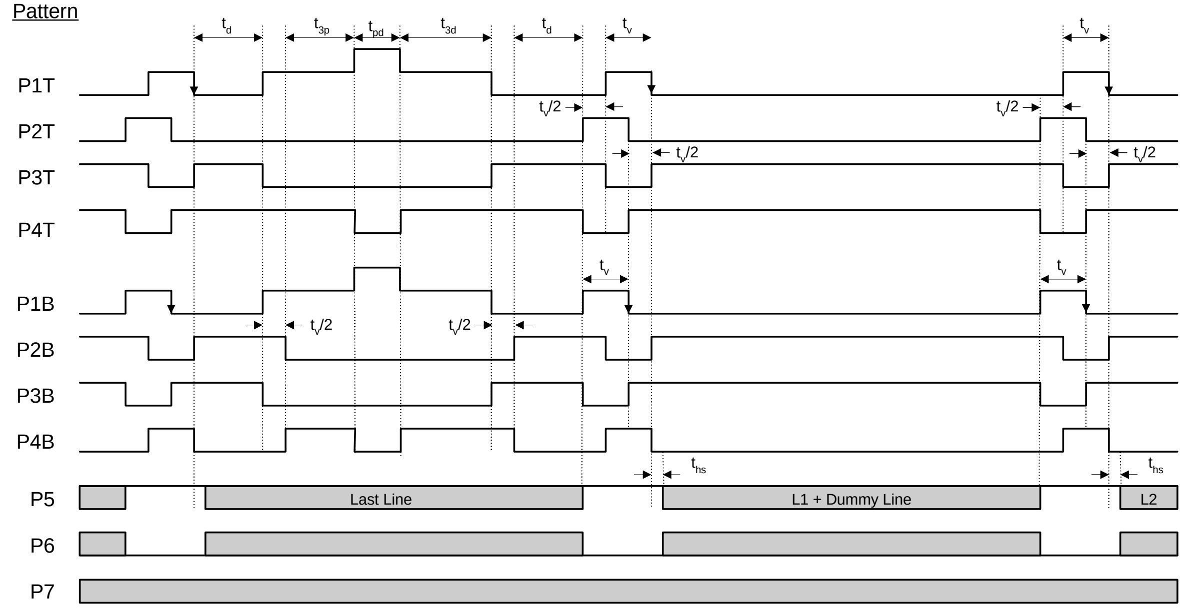

Figure 15: Photodiode Transfer Timing

Line and Pixel Timing

Each row of charge is transferred to the output, as illustrated below, on the falling edge of H2SL (indicated as P6 pattern). The number of pixels in a row is dependant on readout mode – either 1013 or 2026 minimum counts required.

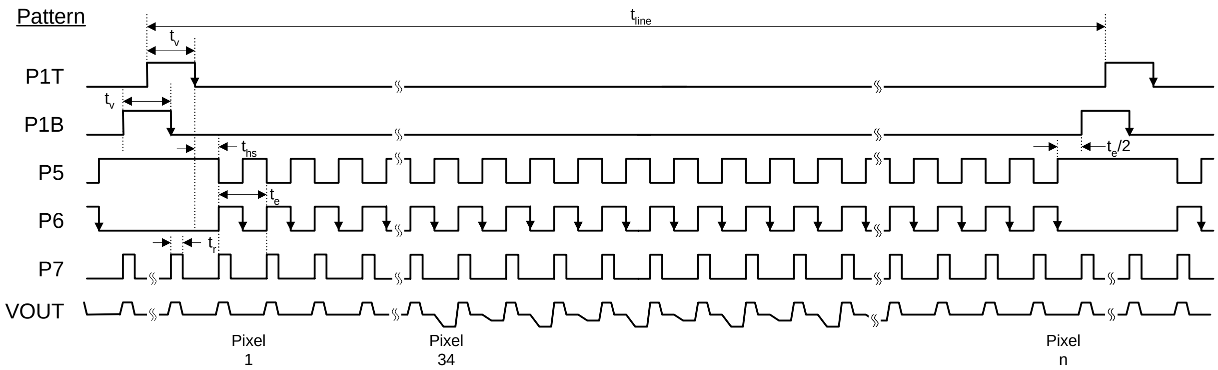

Figure 16: Line and Pixel Timing

Pixel Timing Detail

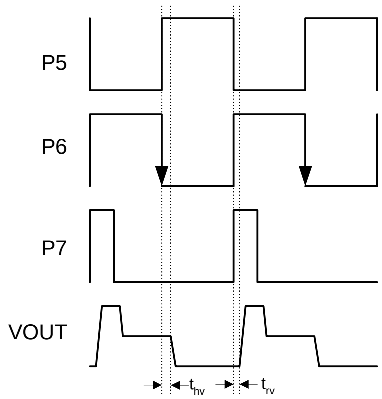

Figure 17: Pixel Timing Detail

Frame/Electronic Shutter Timing

The SUB pin may be optionally clocked to provide electronic shuttering capability as shown below. The resulting photodiode integration time is defined from the falling edge of SUB to the falling edge of V1 (P1 pattern).

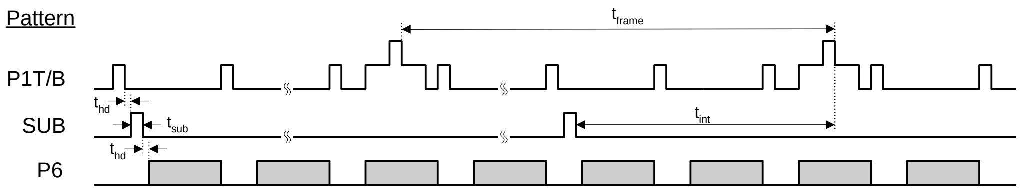

Figure 18: Frame/Electronic Shutter Timing

VCCD Clock Edge Alignment

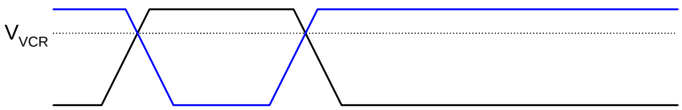

Figure 19: VCCD Clock Edge Alignment

Line and Pixel Timing – Vertical Binning by 2

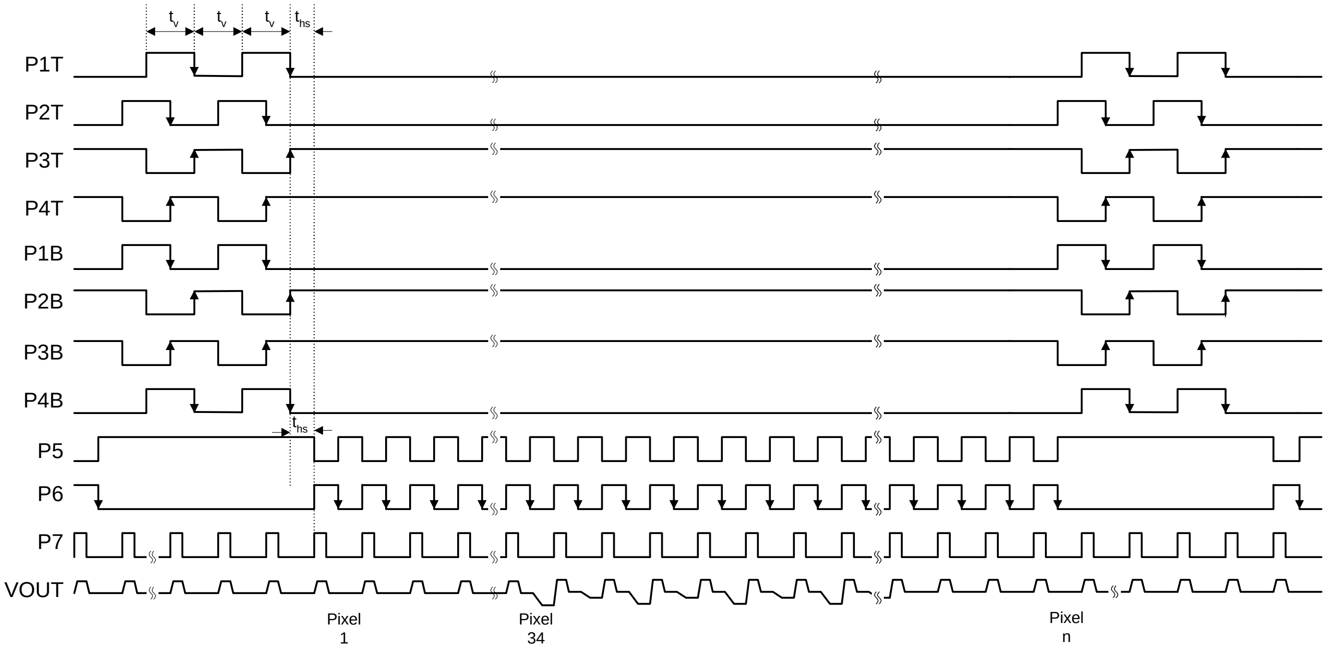

Figure 20: Line and Pixel Timing - Vertical Binning by 2

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STORAGE AND HANDLING

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-55	+80	° C	1
Humidity	RH	5	90	%	2

Notes:

1. Long-term storage toward the maximum temperature will accelerate color filter degradation.
2. T=25° C. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). CCD image sensors can be damaged by electrostatic discharge. Failure to do so may alter device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices" for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices"

ENVIRONMENTAL EXPOSURE

1. Do not expose to strong sun light for long periods of time. The color filters and/or microlenses may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter/microlens aging.
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases. Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370°C. Failure to do so may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

MECHANICAL INFORMATION

COMPLETED ASSEMBLY

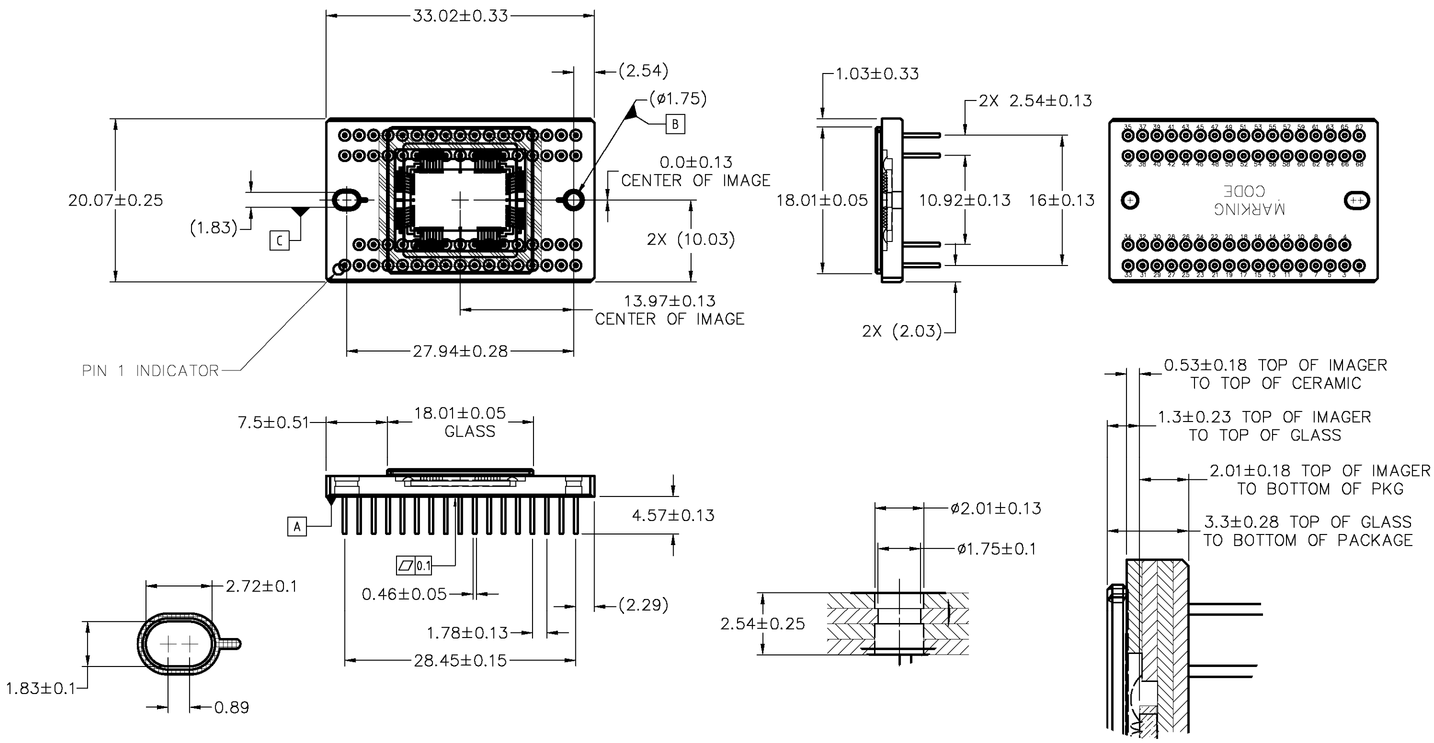

Figure 21: Completed Assembly

Notes:
1. See Ordering Information for marking code.
2. No materials to interfere with clearance through guide holes.
3. The center of the active image is nominally at the center of the package.
4. Die rotation < 0.5 degrees
5. Glass rotation < 1.5 degrees
6. Internal traces may be exposed on sides of package. Do not allow metal to contact sides of ceramic package.
7. Recommended mounting screws:
   1.6 X 0.35 mm (ISO Standard)
   0 – 80 (Unified Fine Thread Standard)
8. Units: IN [MM]

COVER GLASS

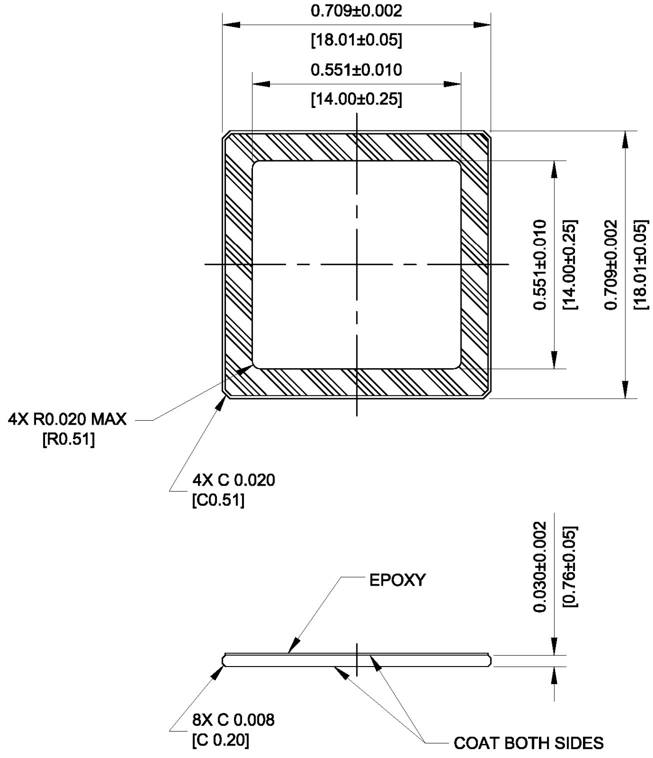

Figure 22: Cover Glass

Notes:

1. Dust/Scratch count – 12 micron maximum
2. Units: MM

COVER GLASS TRANSMISSION

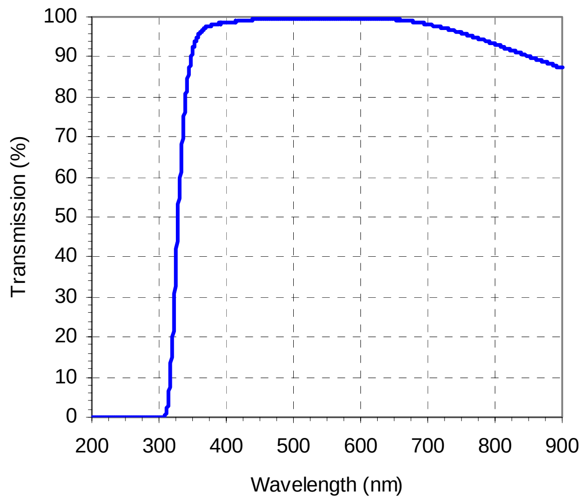

Figure 23: Cover Glass Transmission

QUALITY ASSURANCE AND RELIABILITY

QUALITY STRATEGY

All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note "Quality and Reliability" (MTD/PS-0292).

REPLACEMENT

All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

LIABILITY OF THE CUSTOMER

Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

RELIABILITY

Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note "Quality and Reliability" (MTD/PS-0292).

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

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REVISION CHANGES

Revision Number	Description of Changes
1.0	• Initial formal release

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